

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

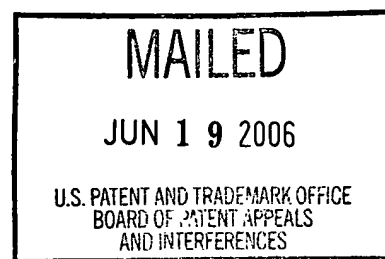
UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAMES D. DWORKIN and MICHAEL J. TORLA

Appeal No. 2006-0910
Application No. 09/725,821

ON BRIEF



Before THOMAS, RUGGIERO, and MACDONALD, Administrative Patent Judges.
RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 1-8 and 14-18, which are all of the pending claims in this application. Claims 9-13 have been canceled. An amendment filed June 20, 2005 after final rejection has been approved for entry by the Examiner.

The claimed invention relates to the selective processing of first and second hash algorithms in which a function circuit

receives first, second, and third chaining variables from a register file. A multiplexer receives a fourth chaining variable when a first hash algorithm is being processed and receives a zero value when a second hash algorithm is being processed.

Claim 1 is illustrative of the invention and reads as follows:

1. An apparatus for selectively processing first and second cryptographic hash algorithms, comprising:

a register file (12) having at least five registers for storing chaining variables;

a function circuit (22) receiving first (B), second (C) and third (D) chaining variables and an output that provides a logical data value;

a first multiplexer (24) having an input coupled to the register file for receiving a fourth (E) chaining variable and an output that provides the fourth chaining variable when the first cryptographic hash algorithm is being processed by the apparatus and a zero value when the second cryptographic hash algorithm is being processed by the apparatus; and

a summing circuit (30) having a first input coupled to the output of the function circuit for receiving the logical data value, a second input coupled to the output of the first multiplexer, and an output coupled to the register file.

The Examiner relies on the following prior art:

Batcher	4,314,349	Feb. 02, 1982
Niehaus et al. (Niehaus)	4,399,517	Aug. 16, 1983
Masaki	4,739,195	Apr. 19, 1988
Turner et al. (Turner)	4,896,296	Jan. 23, 1990
Childs et al. (Childs)	5,623,545	Apr. 22, 1997

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Ober et al. (Ober) 6,708,273 Mar. 16, 2004
(filed Feb. 25, 1999)

Bruce Schneier (Schneier), Applied Cryptography: Protocols, Algorithms and Source Code in C, 436-41, (2nd ed., New York, John Wiley & Sons, 1996).

Claims 1-8 and 14-18, all of the appealed claims, stand finally rejected under 35 U.S.C. § 103(a). As evidence of obviousness, the Examiner offers the combination of Ober, Childs, Schneier, Turner, and Batchner with respect to claims 1-7, 14, 15, 17, and 18, adds Niehaus to the basic combination with respect to claim 8, and adds Masaki to the basic combination with respect to claim 16.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs¹ and Answer for their respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the Examiner and the evidence of obviousness relied upon by the Examiner as support for the rejections. We have, likewise, reviewed and taken into

¹ The Appeal Brief was filed August 19, 2004. In response to the Examiner's Answer mailed November 22, 2004, a Reply Brief was filed January 28, 2005 which was acknowledged and entered by the Examiner as indicated in the communication mailed March 9, 2005.

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consideration, in reaching our decision, Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1-8 and 14-18. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. Rudkin-Wiley Corp., 837 F.2d

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1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

With respect to the Examiner's 35 U.S.C. § 103(a) rejection of appealed independent claims 1 and 14 based on the combination of Ober, Childs, Schneier, Turner, and Batchner, Appellants assert that the Examiner has failed to set forth a prima facie case of obviousness since proper motivation for the proposed combination of references has not been established. After reviewing the arguments of record from Appellants and the Examiner, we are in general agreement with Appellants' position as stated in the Briefs.

The Examiner proposes (Answer, page 4) to provide a hardware implementation of the hash algorithm processing device of Ober as modified by Childs and Schneier by utilizing the selective input multiplexing teachings of Turner and the generalized use of

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multiplexers suggested by Batchner. In our view, however, the programmable logic device of Turner has little relevance to the hash algorithm processors of Ober, Childs, and Turner and, at best, provides only a disclosure that selective input multiplexers may be known in the art. Similarly, our review of the disclosure of Batchner, which is directed to a parallel array processors, reveals nothing more than a teaching that the number of circuit elements may be reduced by utilizing multiplexers.

Given the above discussed deficiencies in the applied prior art, we fail to see how and in what manner the Ober, Childs, and Schneier references might have been modified by Turner and Batchner to arrive at the features set forth in appealed independent claims, each of which requires a specific combination of chaining variable registers and a function circuit coupled to a multiplexer to deliver specific outputs dependent on a particular hash algorithm being processed. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F. 2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). In our view, given the disparity of problems addressed by

the applied prior art references, and the differing solutions proposed by them, any attempt to combine them in the manner proposed by the Examiner could only come from Appellants' own disclosure and not from any teaching or suggestion in the references themselves.

We have also reviewed the Masaki reference applied by the Examiner to address the exclusive-OR circuitry feature of dependent claim 16. We find nothing, however, in the disclosure of the Masaki reference which would overcome the innate deficiencies of the Ober, Childs, Schneier, Turner, and Batcher references as discussed supra.

In view of the above discussion, since we are of the opinion that the proposed combination of references set forth by the Examiner does not support the obviousness rejection, we do not sustain the rejection of independent claims 1 and 14, nor of claims 2-7 and 15-18 dependent thereon.


We also do not sustain the Examiner's obviousness rejection of independent claim 8 in which the Niehaus reference is added to the proposed combination to address the claimed adder circuit feature. As with the Masaki reference, we find nothing in Niehaus which overcomes the previously discussed deficiencies of

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Ober, Childs, Schneier, Turner, and Batcher.

In summary, we have not sustained the Examiner's rejections of any of the claims on appeal. Therefore, the decision of the Examiner rejecting claims 1-8 and 14-18 under 35 U.S.C. § 103(a) is reversed.

REVERSED


JAMES D. THOMAS)
Administrative Patent Judge)
)

Joseph F. Ruggiero
JOSEPH F. RUGGIERO
Administrative Patent Judge

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ALLEN R. MACDONALD
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